ABSTRACT OF THE DISCLOSURE

A device and method to detect and correct for clock duty cycle skew in a high performance microprocessor having a very high frequency clock. The device includes a delay chain circuit to delay the clock signal and to determine the presence of clock duty cycle skew. The device uses simple latches, flops, and phase-detectors to compare and identify the nature of the clock duty cycle skew. Simple logic is employed to measure and determine the amount and direction of de-skew to apply to the clock signal. After the de-skew operation, the clock duty cycle cycles used to control the execution of the microprocessor are of a more uniform time duration.

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